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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,865	09/18/2003	Min-Su Kim	5484-110	8456

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,865	KIM, MIN-SU	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 18 September 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/096,185.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/18/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,424,011 to Assaderaghi et al. in view of U.S. Patent No. 5,767,549 to Chen et al.

Claims 1 and 4, although not directly in a product-by-process form, present an implied methodology of forming an opening portion in an insulating layer, and then filling the opening with a metal to form the local interconnect structure. The final product as claimed, however, is not distinguishable from a product made by a different ordering of steps, however, such as providing a patterned metal portion first, and then disposing a dielectric layer around the patterned metal portion. Note that "determination of patentability in 'product-by-process' claims is based on product itself, even though such claims are limited and defined by process, and thus product in such claim is unpatentable if it is the same as, or obvious form, product of prior art, even if prior product was made by a different process", *In re Thorpe, et al.*, 227 USPQ 964 (CAFC 1985). For the purposes of examination, the limitations of having an opening in the dielectric layer, and having an LIC filled with conductive material in the opening are only accorded weight insofar as they affect the claimed final product.

Regarding claims 1 and 4, Assaderaghi discloses a SOI substrate comprising: a silicon substrate, a BOX layer, and an SOI layer (figures 5a-5l); a well (SOI islands are wells; see figure

5e) such that a lower surface of the well is in contact with the BOX layer (figure 5e); a field oxide film (202) formed adjacent to the well (figure 5a); a gate line ("n-gate"; see figures 7b and 8b) connected across an active area (source, drain, and channel regions in figures 7b, 8b) and a portion of the field oxide (see figure 8b; field oxide surrounds active region), the active area formed along two sides of the gate line and having a lower surface in contact with the BOX (active region is SOI region; see figures 5e, 7b); an insulation layer (211, 217; since the layers are not different materials, they can be considered "an insulating layer") formed on the active area, gate line, and field oxide film (figure 5f-5h); an opening part formed within the insulation layer (portion filled with plugs 212 and wires 213; see figure 5f), the opening part opened in a full trench partially exposing an active area of an adjacent transistor ('SRAM cell' portion; trench opens to source/drain of the transistor on the right; figures 5f, 5l) and in a partial trench structure to expose an upper part of the gate line (plug above gate line of 'left' transistor connected to source/drain in 'SRAM cell'; see figures 5f, 5g, 5l), and an LIC (interconnection including plugs 212 and wiring 213 in 'SRAM cell') filled with conductive material (212, 213) in the opening part within the insulation layer (both the material 212 for the plugs formed in dielectric layer 211 and the wiring layer 213 in dielectric layer 217 constitute "opening parts" filled with metal formed within an insulating layer).

Assaderaghi fails to disclose that the field oxide film is formed on the surface in a well, such that the lower portion of the well is in contact with the BOX layer, but rather discloses that the field oxide layer extends entirely through the SOI layer.

Chen discloses that it is advantageous for multiple-FET SOI structures to have the field oxide layers (38) formed only on the surface of a well (20), such that the bottom of the well is in contact with the BOX layer (14; see column 1, lines 25-67; column 3, lines 20-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the SOI structure of Assaderaghi, such that the field oxide layer is only provided in the surface of a well, wherein the bottom of the well contacts the BOX layer, as suggested by Chen. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide semiconductor well portions between the buried oxide layer and the field oxide layer, so that floating body effects, which result in lower device gain and kinks in drain current vs. gate voltage (see Chen, column 1, lines 25-50) can be prevented, while eliminating the area penalty and fabrication complexity required for separate body contacts for each device (see Chen, column 1, lines 50-67, column 3, lines 25-40).

Regarding claims 2, 3, 5, and 6, Assaderaghi discloses that the local interconnect comprises tungsten and/or copper (column 6, lines 1-6, 15-20).

3. Claims 1-6 are alternately rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,424,011 to Assaderaghi et al. in view of U.S. Patent No. 5,767,549 to Chen et al. and U.S. Patent No. 6,426,558 to Chapple-Sokol et al.

The teachings of Assaderaghi and Chen as applied to claims 1 and 4 are presented supra.

If it is alternately assumed that the implied method steps of forming an opening part in the insulation layer, and filling the opening part to form an LIC, do affect the final structure and

have patentable weight, Assaderaghi as modified by Chen fails to teach a monolithic LIC structure having an opening portion in a dielectric layer, where the opening portion contacts a gate in a partial trench and impurity region in a full trench, where the entire structure is filled with a metal to form the LIC.

Chapple-Sokol discloses that it is known in the art and advantageous to use a monolithic interconnect structure including a partial-trench gate contact (figures 13-17; at gate 14), a full trench contact to an impurity region (at left side of figures 13-17), and an interconnection portion between the two (44). Chapple-Sokol further teaches that copper and tungsten can be used as metal fill materials (column 5, line 58-column 6, line 25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the SOI structure of Assaderaghi as modified by Chen, such that it uses a monolithic LIC structure, as taught by Chapple-Sokol. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a monolithic LIC structure with copper or tungsten fills, because doing so reduces device yield problems associated with the seam between the plugs and wiring layers (Chapple-Sokol, column 1, lines 35-55) and simplifies the fabrication process for forming the LIC structures (Chapple-Sokol, column 2, lines 23-45; column 5, line 35- column 6, line 35). Furthermore, a person skilled in the art would have been motivated to use tungsten or copper for the fill, because such materials have high conductivity and are suitable for use as interconnection materials.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent Publication No. 2002/0003241 to Kuriyama discloses an SRAM structure having local interconnects, but fails to provide the specified SOI substrate.

b. U.S. Patent Publication No. 2002/0020878 to Kawanaka discloses local interconnect structures for an SOI, but does not teach a LIC connecting a gate and a source/drain of an adjacent transistor.

c. U.S. Patent No. 6,627,952 to Wollesen discloses local interconnects for an SOI with 'shallow' field oxide portions, but does not teach the specifics of the LIC.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

ERIK KIELIN
PRIMARY EXAMINER